ISSN (Print) : 2319-5940
ISSN (Online) : 2278-1021

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 2, Issue 3, March 2013

HIGH PERFORMANCE DADDA MULTIPLIER IMPLEMENTATION USING HIGH SPEED CARRY SELECT ADDER

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Abstract: Two well known fast multipliers are those presented by Dadda and Wallace. Both multipliers use full adders and half adders in their reduction phase. The half adder does not reduce the number of partial product bits. Therefore minimizing the number of half adders in the multiplier will reduce the complexity. In the modified Wallace tree number of half adders is reduced to 80 percent. In Wallace multiplier the partial products are reduced as soon as possible. Therefore more number of half adders and full adders is required. But in Dadda multiplier reduction is performed whenever necessary. In the final carry propagation path carry select adder is used. A Carry Select Adder using BEC is introduced but it offers some speed penalty. This paper proposes an efficient carry select adder using D Latch.

Keywords: BEC, Dadda, Wallace, Modified Wallace, CSA

1. INTRODUCTION

Two well known fast multipliers are those presented by Wallace[1][3] and Dadda[2]. Both of these multipliers consist of three stages. In the first stage, partial product matrix is formed. In the second stage, partial product matrix is reduced to a height of two. In the final stage, these two rows of partial products are combined using carry propagation adder. In the Wallace method the partial products are reduced as soon as possible. But in Dadda multiplier perform the minimum reduction at each level. Wallace and Dadda multipliers use full adders and half adders in their reduction stage. In the Wallace multiplier partial product reduction is performed as soon as possible. So the number of half adders and full adders required for the partial product reduction in Wallace multiplier is high. But the half adders does not reduce the number of partial product bits. So a modification to the Wallace reduction is presented which reduce the number of half adders. But in Dadda multiplier less number of half adders are required than the Wallace and Modified Wallace multiplier. For an N bit Wallace multiplier the number of half adders required is $N^{1.5}$ and for an N bit Dadda multiplier the number of half adders required is N-1.
For the final carry propagation adder we use Carry select adder. Carry select adder having Binary to

Excess one converter in its basic structure is available. But it offer some speed penalty. This disadvantage can be overcome by using D Latch instead of BEC.

1. DADDA MULTIPLIER

Dadda multipliers are the refinement of parallel multipliers first presented by Wallace in 1964. In contrast to the Wallace reduction Dadda multiplier perform the least reduction at each stage[4]. The maximum height of each stage is determined by working back from final stage

which consists of two rows of partial products. The height of each stage should be in the order 2, 3, 4,6,9,13,19,28,42,63 etc. An 8 bit Dadda multiplier reduction is shown in figure 1.

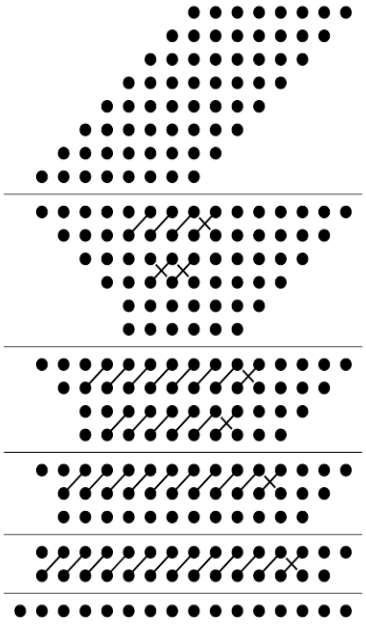

Figure 1.Dadda Multiplier for N=8

ISSN (Print) : 2319-5940
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For Dadda multipliers the number of full adders and half adders required depends on the value of N.

No of Full Adders = N^2-4N+3
No of Half Adders = N-1

2. WALLACE MULTIPLIER

In the conventional Wallace Tree multiplier the partial products are formed by N2 AND gates in the same manner as that of Dadda multiplier. The formed partial products are collected to group of three or two. Full adders are applied to columns containing three bits and half adders to column containing two bits. Carry save adders are used for the addition of partial products[5]. Since the Wallace multiplier performs the reduction as soon as possible the number of half adders and full adders required is high. The conventional Wallace multiplier for N=8 is shown in figure 2.

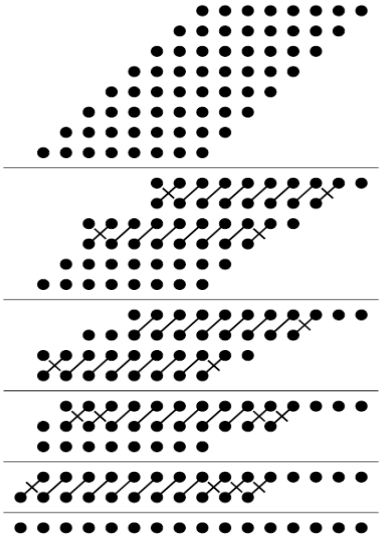

Figure 2.Wallace Multiplier for N=8

3. MODIFIED WALLACE MULTIPLIER

The Modified Wallace multiplier is similar to that of Conventional Wallace multiplier in that it uses as many full adders as possible, but different in that it only use half adders when necessary to ensure that the number of reduction stage is same as for Conventional Wallace Tree multiplier[6].

The Modified Wallace Tree at first make the partial product formed into the pyramidal structure and divide the structure into tree rows of group and uses full adders for each group of three bits in a column. A group of three bits in a column is not processed, that is, it is passed on to the next stage. Single bits are passed on to the next stage as in the conventional Wallace reduction.

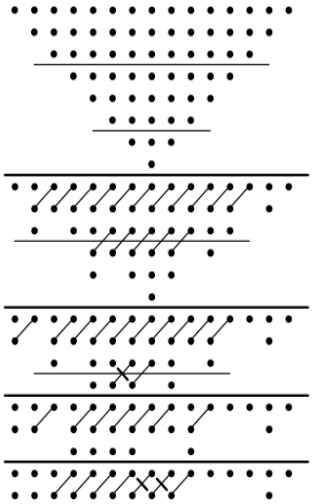

Figure 3. Modified Wallace for N=8

4. CARRY PROPAGATION ADDER

4.1 CARRY SELECT ADDER USING D LATCH

In the previous works hybrid adders are used for the final carry propagation part. The hybrid adders consist of carry look ahead adder and carry select adder. But carry select adder takes more area. So carry select adder which include BEC (Binary to Excess One converter) in its structure is included[6]. But it offers some speed penalty. In this structure the RCA with carry input equal to one is replaced by BEC. The structure of BEC for five inputs is given in figure 3.

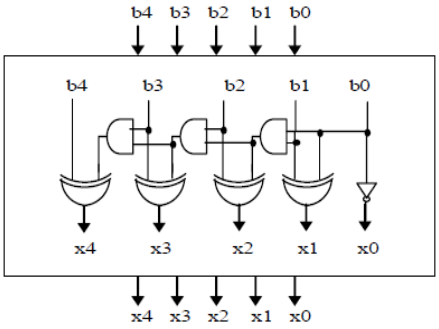

Figure 4. 5 bit Binary to Excess One Converter

In the proposed architecture this BEC is replaced by D Latch which avoids the speed penalty introduced by BEC. In the carry select adder structure using D Latch the sum and carry for cin=0 and cin=1 is calculated within the one clock cycle itself. The basic structure of carry select adder using D Latch is shown in figure 5.

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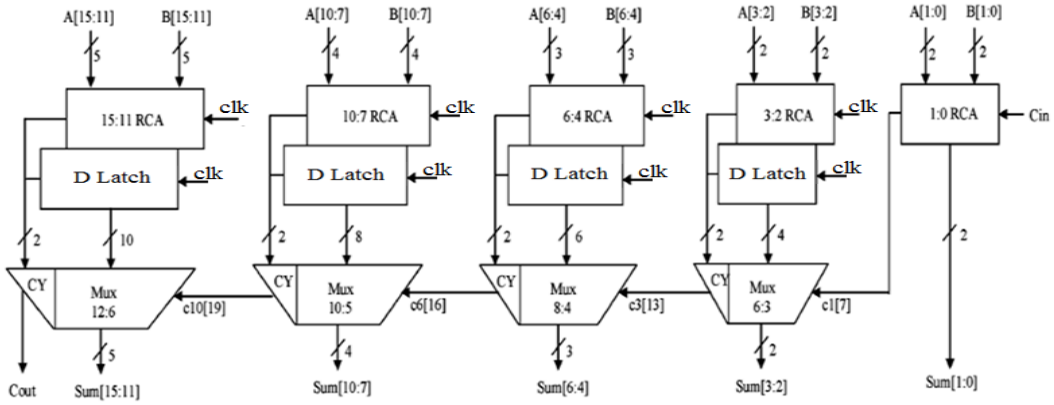

Figure 5.Carry Select Adder using D Latch

This is a 16-bit adder in which least significant bit adder(LSB) is a ripple carry adder, which is two bit wide. The upper half of the adder is 14 bit wide which work according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in the adder itself. The latch is used to store sum and carry for cin=1. The carry out from the previous stage is used as control signal for multiplexer to select final output carry and sum. Cout is the final output carry. Figure 6 shows the internal structure of group 2 of the proposed 16 bit carry select adder. The group 2 performed the two bit addition which are a2 with b2 and a3 with b3. This is done by two full adders named FA2 and FA3 respectively. The third inut to the full adder FA2 is clock instead of carry and third input to the full adder FA3 is the carry output from the FA2. The group 2 structure has three D Latches in which two are used for storing the su2 and sum3 from FA2 and FA3 and the last one is used to store carry. Multiplexer is used for selecting sum and carry according to the carry coming from the previous stage.

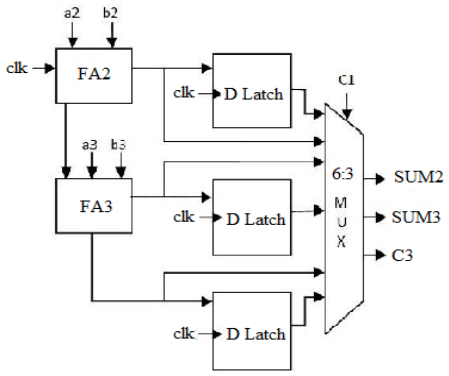

Figure 6. Group 2

5. SIMULATION RESULTS

The number of full adders and half adders required for Wallace, Modified Wallace and Dadda multiplier is shown in Table 1.

Table 1. Complexity of reduction

Input size	8	16	32	64
WALLACE				
FA	38	200	906	3850
HA	15	52	156	430
TOTAL GATES	402	2008	8788	36388
MOD WALLACE				
FA	39	201	907	3853
HA	3	9	23	53
TOTAL GATES	363	1845	8263	34889
DADDA				
FA	35	195	899	3843
HA	7	15	31	63
TOTAL GATES	343	1815	8215	34839

The comparison result of Wallace, Modified Wallace and Dadda multiplier using carry select adder using BEC and carry select adder using D Latch in the final carry propagation part is shown in Table 2. The comparison results shows that among all the multipliers Dadda multipliers having carry select adder using D Latch in its carry propagation path is more efficient.

Table 2. comparison results of multipliers

Multiplier	Bit	Devices		Delay(ns)	
		BEC	D Latch	BEC	D Latch
WALACE	8bit	248	249	36.4	25.8
	16bit	646	659	54.7	52.9
MOD WAL	8bit	143	144	31.2	25.2
	16bit	596	602	54.3	52.5
DADDA	8bit	137	138	25.1	24.0
	16bit	569	580	51.5	47.4

By using carry select adder using D Latch in the final carry propagation path instead of carry select adder with BEC the speed can be increased.

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Table 3. Comparison result of adders

Parameters	CSA using BEC(16 bits)	CSA using D Latch(16 bits)
Delay(ns)	23.287	21.488
Power(mW)	650.42	650.51

6. CONCLUSION

In this paper a modification to the Wallace multiplier is performed. The comparison result shows that the modified one reduces the number of half adders by 80%. But Wallace and Modified Wallace reduction use more gates for their reduction than Dadda multiplier. CSA with BEC and CSA with D Latch is introduced in the final carry propagation path of the multipliers. From all the comparison results we can conclude that the Dadda multiplier with CSA with D Latch in the final carry propagation path is more efficient.

ACKNOWLEDGEMENT

The authors would like to thank to Dr. P. Ramamoorthi, Prof. S. Arumugam, Of the VLSI Division, SNS College of Technology for their contribution of this work.

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